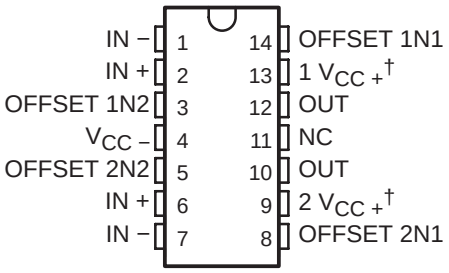
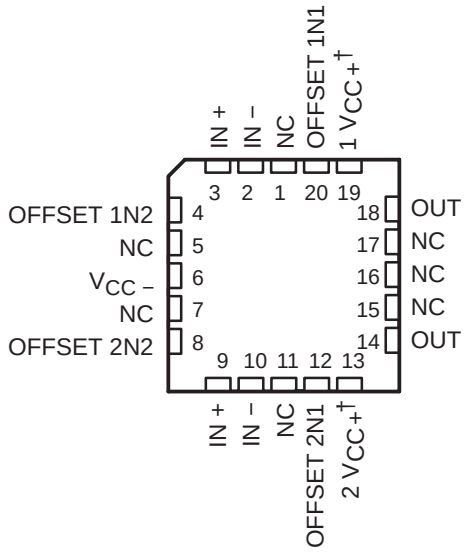
SLOS009A − D971, FEBRUARY 1971 − REVISED OCTOBER 1990

- **No Frequency Compensation Required**
- **Low Power Consumption**
- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Latch-Up**
- **Designed to Be Interchangeable With Fairchild μA747C and μA747M**

D, J, N, OR W PACKAGE
(TOP VIEW)



uA747m . . . FK PACKAGE
(TOP VIEW)



NC − No internal connection

† The two positive supply terminals (1 V_{CC+} and 2 V_{CC+}) are connected together internally.

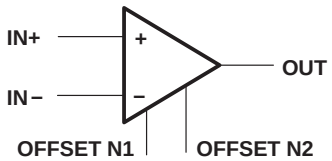
description

The uA747 is a dual general-purpose operational amplifier featuring offset-voltage null capability. Each half is electrically similar to uA741.

The high common-mode input voltage range and the absence of latch-up make this amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The uA747C is characterized for operation from 0°C to 70°C; the uA747M is characterized for operation over the full military temperature range of −55°C to 125°C.

symbol (each amplifier)



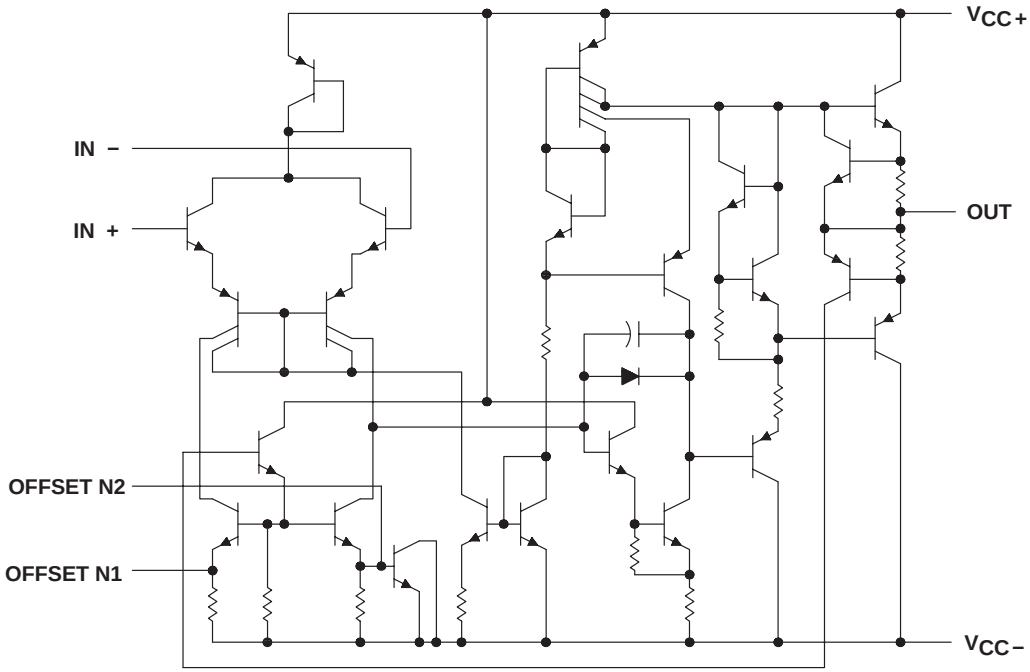
AVAILABLE OPTIONS

T_A	V_{IO} Max AT 25°C	PACKAGE				
		14-PIN				20-PIN
		SMALL OUTLINE (D)	CERAMIC DIP (J)	PLASTIC DIP (N)	FLAT PACK (W)	CHIP CARRIER (FK)
0°C to 70°C	6 mV	uA747CD	—	uA747CN	—	—
−55°C to 125°C	5 mV	—	uA747MJ	—	uA747MW	uA747MFK

The D package is available taped and reeled. Add the suffix R to the device type, (i.e., uA747CDR).

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA747C	uA747M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	22	V
Supply voltage, V_{CC-} (see Note 1)		−18	−22	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage any input (see Notes 1 and 3)		±15	±15	V
Voltage between any offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		0 to 70	−55 to 125	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package		300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260		°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA747M only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	800 mW	7.6 mW/°C	45°C	608 mW	—
FK	800 mW	11.0 mW/°C	77°C	800 mW	275 mW
J	800 mW	11.0 mW/°C	77°C	800 mW	275 mW
N	800 mW	9.2 mW/°C	63°C	736 mW	—
W	800 mW	8.0 mW/°C	50°C	640 mW	200 mW

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS†	T_A‡	uA747C			uA747M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		1	6		1	5	mV
			Full range			7.5			6	
$\Delta V_{IO(adj)}$	Offset voltage adjust range		25°C		±15			±15		mV
I_{IO}	Input offset current		25°C		20	200		20	200	nA
			Full range			300			500	
I_{IB}	Input bias current		25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	24	28		24	28		V
		R_L ≥ 10 kΩ	Full range	24			24			
		R_L = 2 kΩ	25°C	20	26		20	26		
		R_L ≥ 2 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ± 10 V	25°C	25	200		50	200		V/mV
			Full range	15			25			
r_i	Input resistance		25°C	0.3	2		0.3*	2		MΩ
r_o	Output resistance	See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply-voltage sensitivity (ΔV_{IO} / ΔV_{CC})	V_{CC} = ± 9 V to ± 15 V	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (each amplifier)	No load	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Power dissipation (each amplifier)	No load, V_O = 0	25°C		50	85		50	85	mW
			Full range			100			100	
V_{o1}/V_{o2}	Channel separation		25°C		120			120	0	dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡ Full range for uA747C is 0°C to 70°C and for uA747M is −55°C to 125°C.
*On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC\pm}$ = ± 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.3		µs
	Overshoot factor			5%		
SR	Slew rate at unity gain	V_I = 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5		V/µs

PARAMETER MEASUREMENT INFORMATION

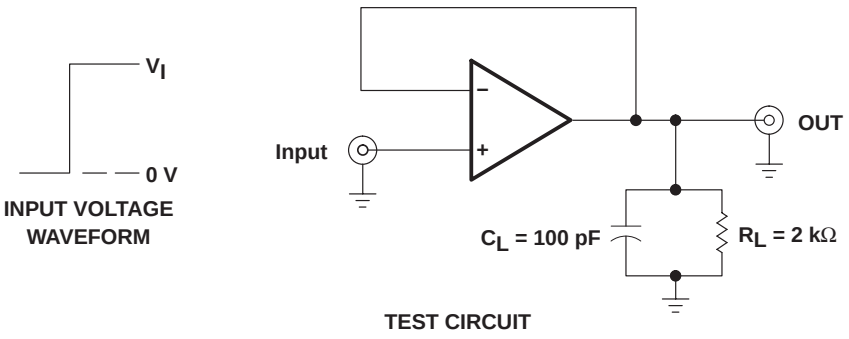


Figure 1. Rise Time, Overshoot, and Slew Rate

APPLICATION INFORMATION

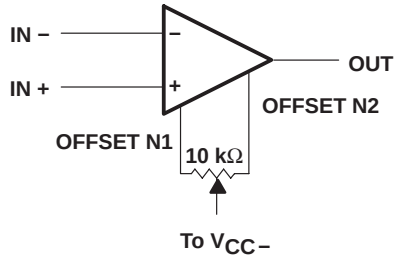


Figure 2. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS†

**INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE**

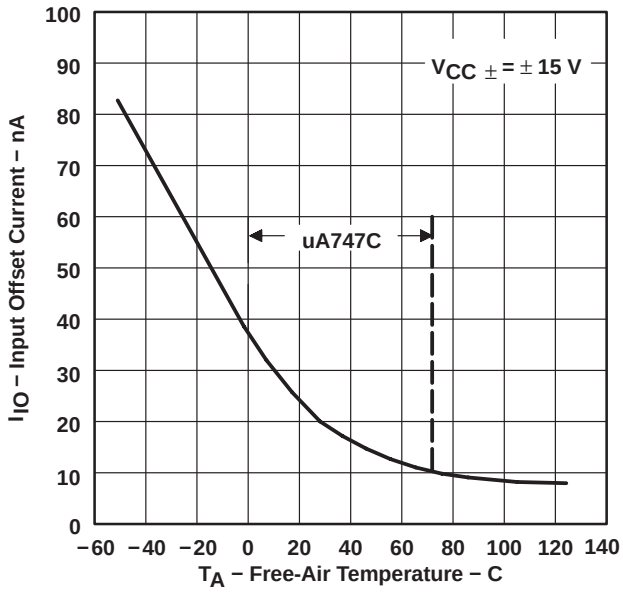


Figure 3

**INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE**

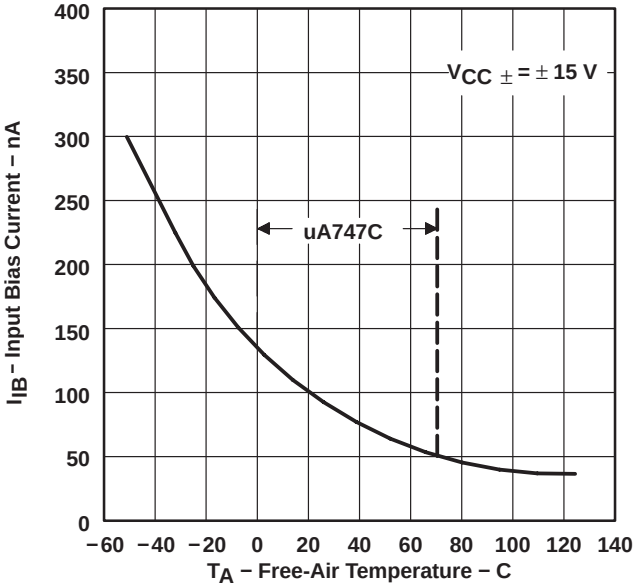


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature range of the particular devices.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

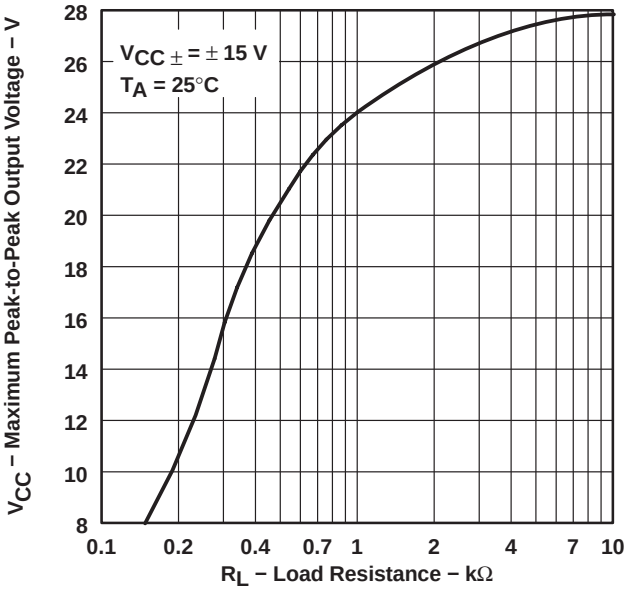


Figure 5

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

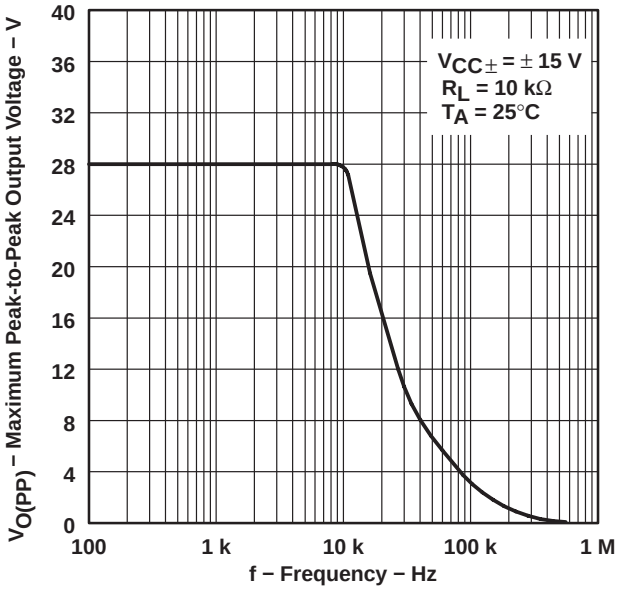


Figure 6

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

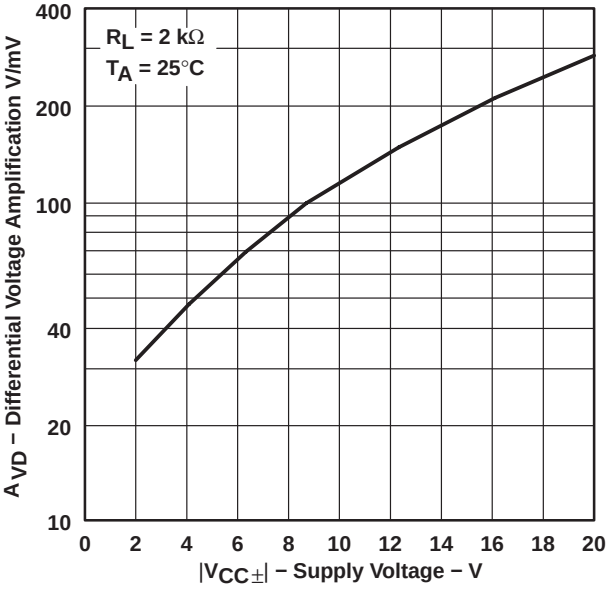


Figure 7

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

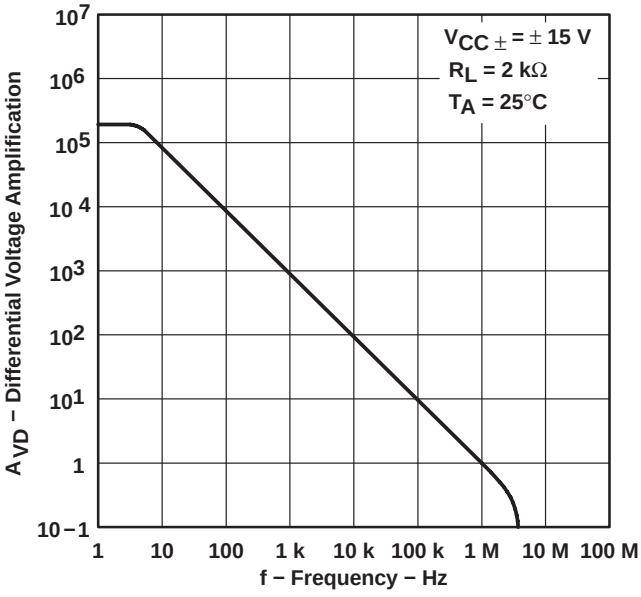


Figure 8

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

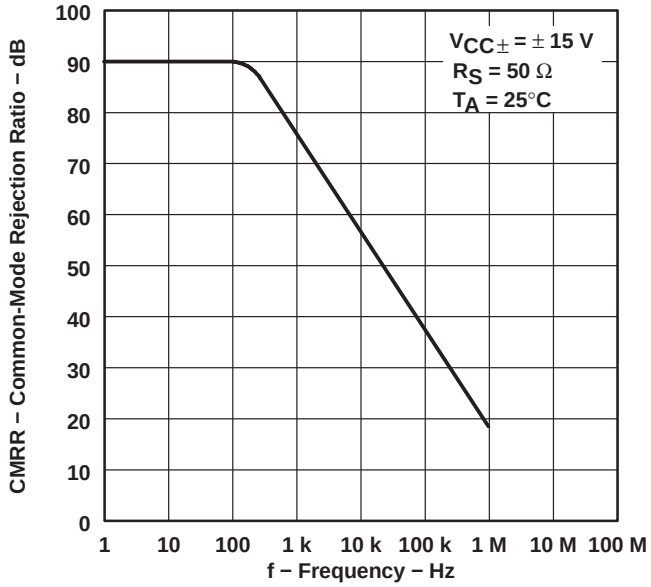


Figure 9

OUTPUT VOLTAGE vs ELAPSED TIME

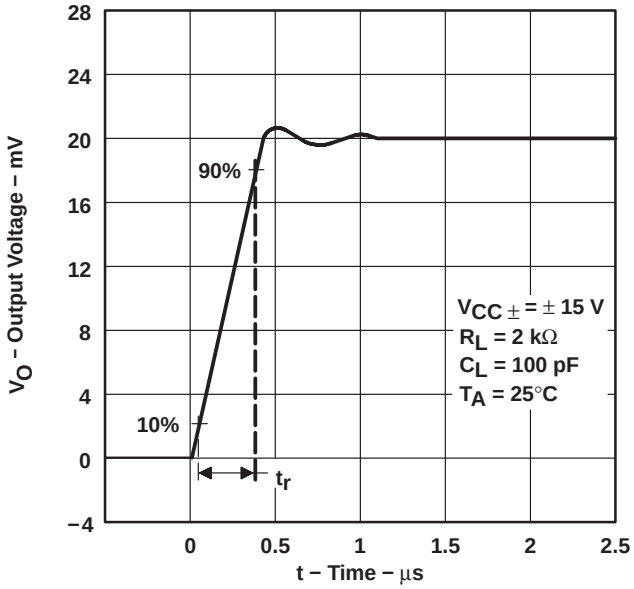


Figure 10

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

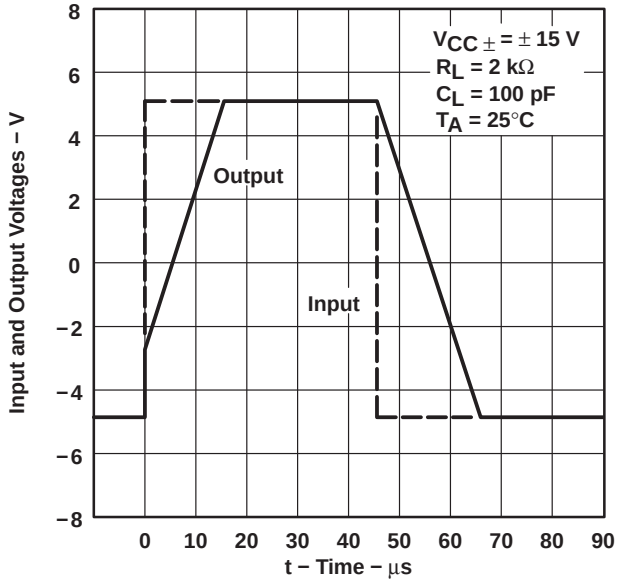


Figure 11

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UA747-1MJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
UA747CD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
UA747CD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
UA747CDR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
UA747CDR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
UA747CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
UA747CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
UA747CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
UA747CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

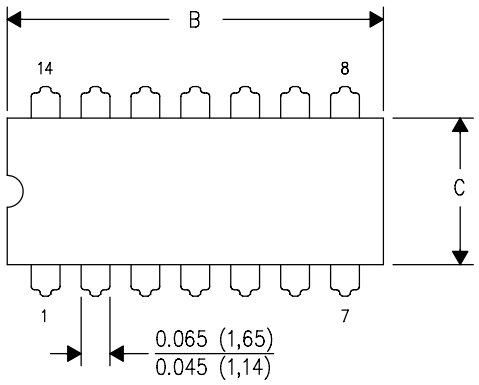
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

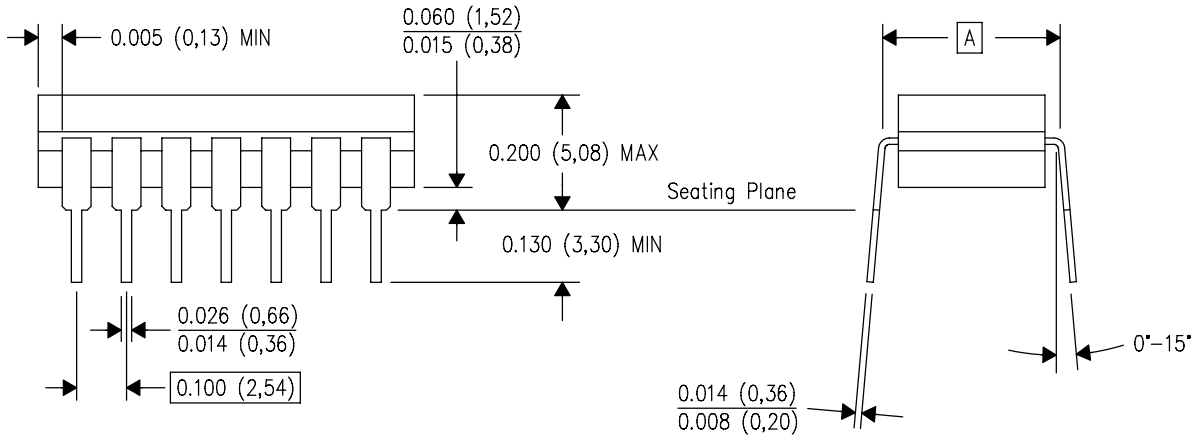
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



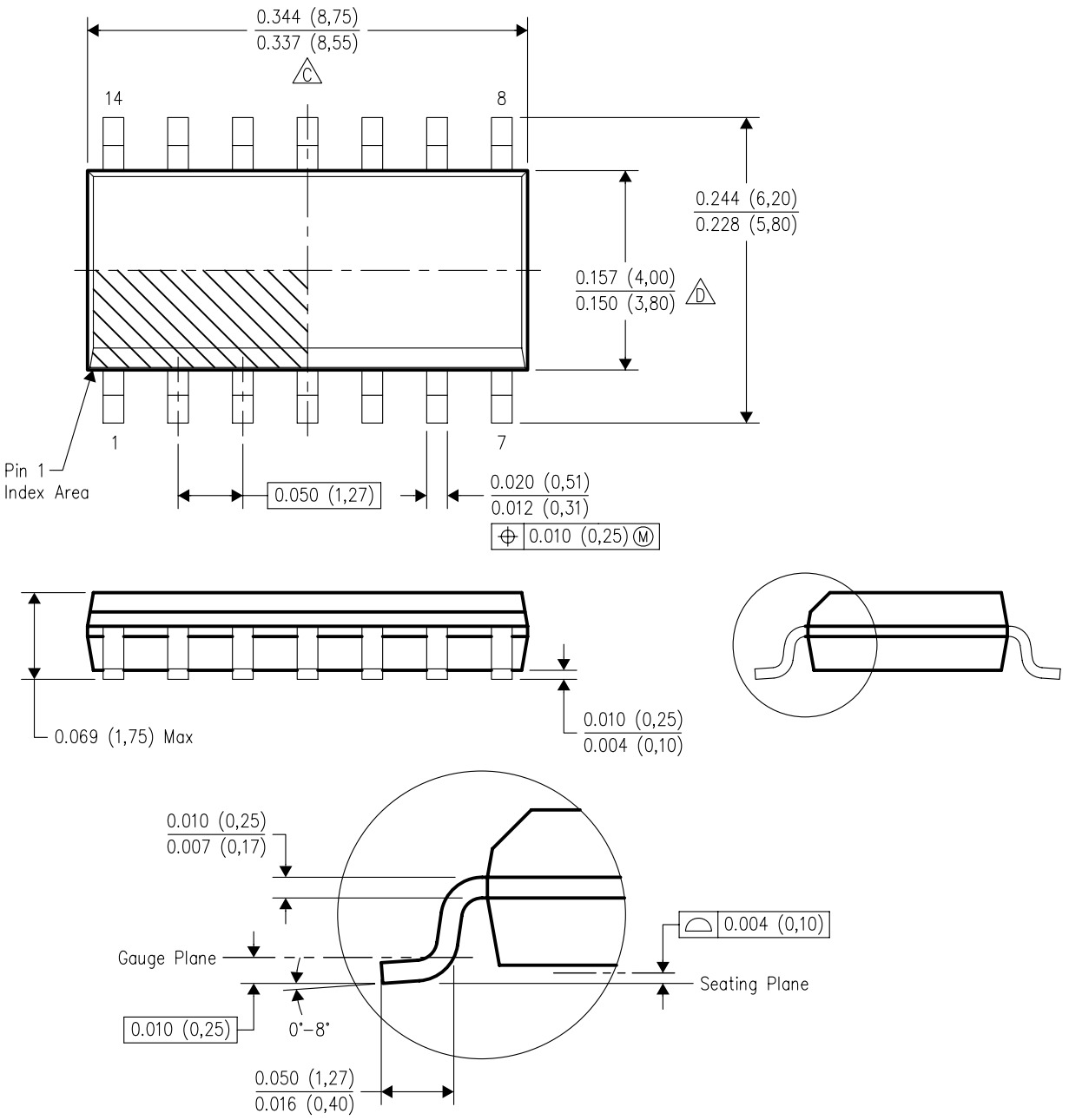
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE

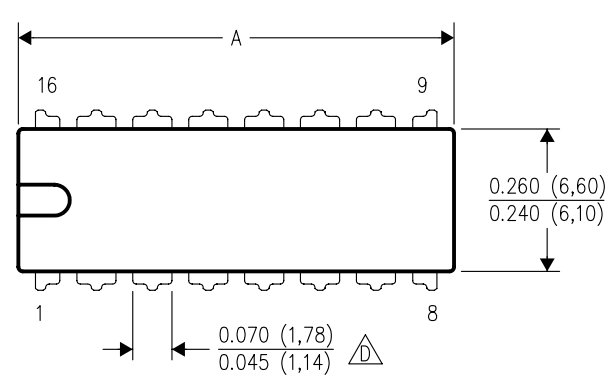


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

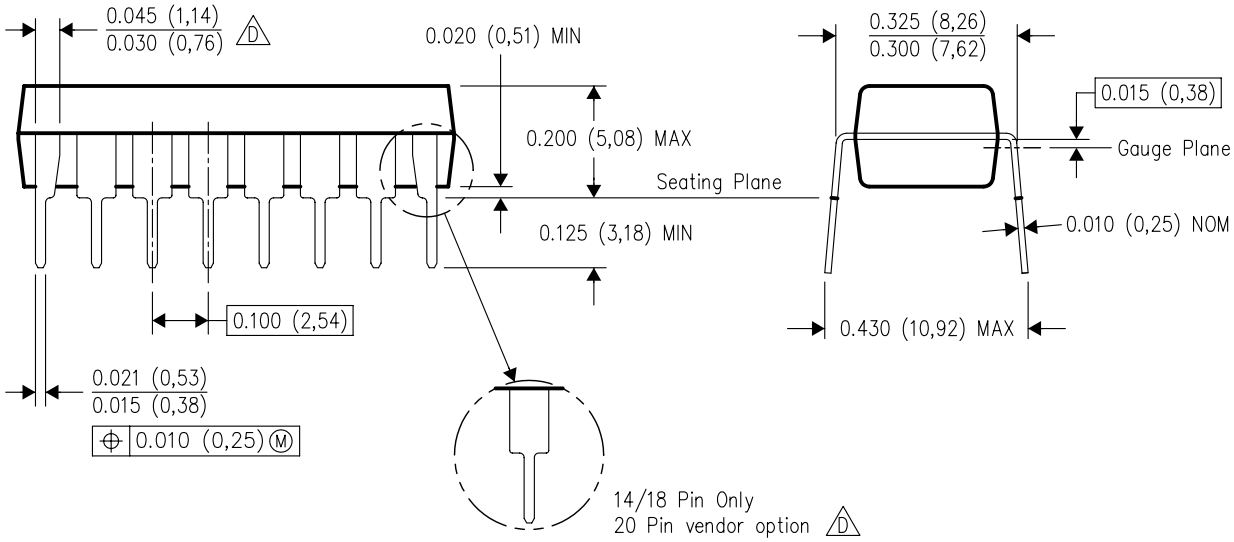
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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